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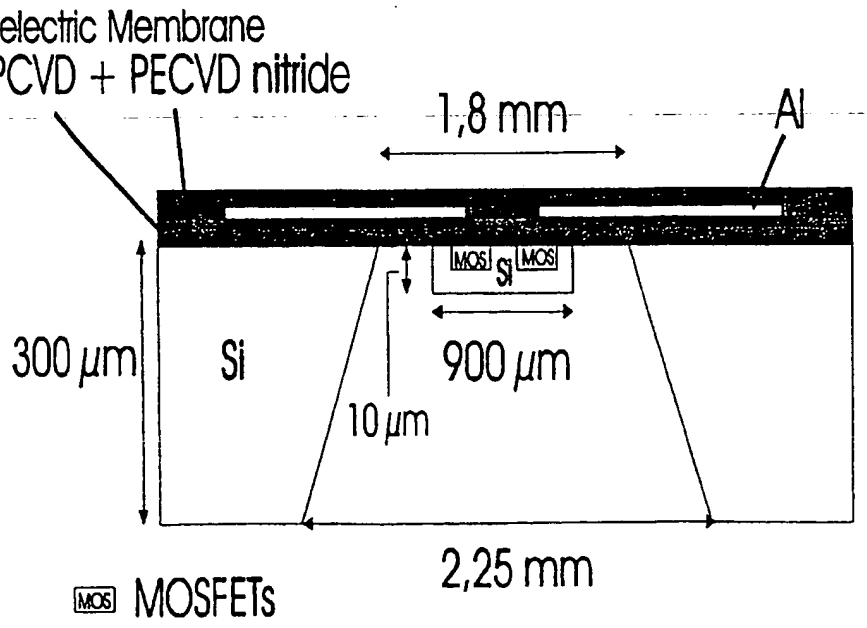
(54) Title: LOW-POWER SENSOR



(57) Abstract: The invented MOSFET array gas sensor has been fabricated using silicon bulk micro machining. A heating resistor, a diode used as temperature sensor and 4 gas-sensitive FETs are located in a silicon island suspended by a dielectric membrane. The membrane has a low thermal conductivity coefficient and therefore thermally isolates the electronic components on the silicon island from the chip frame. This low thermal mass device allows the reduction of the power consumption to a value of 80 mW for an operating temperature of 175 °C. This low power MOSFETs gas sensor array is suitable for applications in portable gas sensors instruments and in automobiles.

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LOW-POWER SENSOR

INTRODUCTION

Gas-sensitive field-effect (GasFETs) devices have been studied for about 25 years. The replacement of the MOSFET gate by materials having catalytic properties (Pt, Pd, Ir...) allows the detection of several gases. During the years, they have shown to be suitable for different applications such as hydrogen monitor and leak detectors and electronic noses. Portable instruments and automotive industry are markets where low-cost and low-power consumption devices are in constant development. During the last years, a lot of work has been done in the gas sensing field on reducing the power consumption of resistive gas sensors devices, but none has been reported on MOSFET type gas sensors. They are when used usually heated to a temperature over 100 °C to increase sensitivity and are limited to 175-200°C due to the use of standard silicon fabrication technologies. The present power consumption for one sensor is about 0.5 to 1.0 W, a major part of which is used to heat the sensor to its working temeperature. A low-power consumption array of GasFETs has been developed to make this technology competitive with the others on these markets.

In view of said comperatively high power consumption it is the object of the invention to lower this for gas-sensitive field-effect (GasFETs) devices.

THE INVENTION

The object of the invention is solved by means of a design and fabrication methodology for micro-machined semiconductor devices comprising "hotplate devices", which makes it possible to combine micro-machining processing with the integration on the hotplate of active microelectronic chemical sensors exposed to the ambient. The device includes a support substrate, a membrane extending over a well in the substrate, and a semiconductor island attached to the membrane and isolated thermally, from the support substrate. The semiconductor island serves as a substrate for the integration of microelectronic chemical sensors, which are exposed to the ambient for instance through a hole in the membrane. The device may include also other active microelectronic components, e.g., circuits for control and sensing, which may be protected by the membrane if required. By including an electric heater and a temperature sensor in the island, a micro-hotplate chemical sensor device is obtained that can be heated under temperature control using very low power. The most important advantage of the disclosed device as compared to traditional devices is that any active microelectronic chemical sensor can be integrated in the hotplate, while still being exposed to the ambient gas or liquid surrounding the device. With the

disclosed device, it becomes possible to utilize chemical sensors based on the so-called field-effect detection mechanism. Field-effect gas sensors have proven to be very useful in many applications, either as single sensors, as arrays consisting of several sensors, or in combination with one or several sensors that utilize a different detection mechanism. By utilizing the disclosed device, it becomes possible to make low-power field-effect gas sensors and sensor arrays. Due to the low thermal mass of the disclosed micro-hotplate devices, the operating temperature of the field-effect gas sensors can be pulsed or varied swiftly in some other way and sensors integrated in the same micro hotplate can be operated at different temperatures. Arrays of multiple sensors can be integrated on the disclosed micro-hotplate together with individual circuits for control and sensing, allowing an independent operation of each individual sensor. Also heating to operating temperatures can be very quick, almost instantaneous. The resulting devices are, e.g., suitable for applications in automobiles, portable gas-sensor instruments, and for on-line measurements using distributed sensor systems.

EMBODIMENT

Further advantages and developments of the invention are apparent from the claims as well as from the following description of an embodiment with reference to the Fig 1 in the drawings, depicting a cross section of an embodiment of the invention, it should be noted that the cross section is very much enlarged and not to scale since the dimensions in the vertical direction (as viewed) is enlarged many times more than the horizontal direction for improved illustration. Fig 2 shows a similar device somewhat simplified and fabricated in accordance with claim 13. Fig 3 illustrates yet another way to fabricate a micro-hotplate, this time in accordance with claim 15. In fig 4 a micro-hotplate made in accordance with claim 16 is shown. Fig. 5 is a cross section of a device similar to fig 1, but where the sensor is contactable by for instance ambient gas in a more direct manner.

Sensor chip

The MOSFETs array gas sensor realized (fig. 1) has been designed in the aim of reducing the source and drain leakage currents and the power consumption of this type of gas sensors. Each device consists of 4 GasFETs, a temperature sensor (diode) and a heater. The actual chip size is $4.0 \times 4.0\ mm^2$.

Electronic components

The heater is a semiconducting resistor, which is made during the p-well implantation of the MOSFET fabrication process. The transistors (NMOS) and the diode temperature sensor are made in a single diffusion step of doping atoms from CVD oxide films. Arrays with 4 medium or small MOSFETs have been designed respectively with a channel length of 13.0 and 5.0 μm. The fabrication of NMOS transistors in a p-well technology allows to drive them separately. Their source/drain leakage currents have been limited by minimizing the p-n junction surface at the source and the drain regions. Therefor, the metal / semiconductor contacts are directly taken on the source and the drain just beside the gate. GasFETs operate with their drain and gate connected together with a constant current bias between the source and the drain. In this design, the drain and gate were not connected together to allow more flexibility during the characterization of the MOSFETs electrical properties.

Power consumption

The thermal mass and therefore the power consumption of the sensor are minimized by the design. The GasFETs, the heater and the diode are located in a silicon island isolated from the chip frame by a dielectric membrane. The membrane is made of LPCVD low-stress silicon nitride. A PECVD silicon nitride film is used as a passivation layer on the aluminum metallization. The membrane size is 1.8 x 1.8 mm^2 and the silicon island area is 900 x 900 μm^2 and 10 μm thick.

FABRICATION

Three main parts compose the fabrication process:

1. Fabrication of the doped regions in the silicon to make the electronic components;
2. Gate oxide growth and deposition of the membrane, the metallization, and passivation films; and
3. Release of the membrane and the formation of the silicon island by for instance wt anisotropic etching of silicon.

Electronic components

The process starts with the implantation of boron in a 4" silicon substrate (25 Ωcm, n type,

300 μm thick double face polished) to form the MOSFETs p-well, the p side of the diode and the resistive heater. Also included in this first part is the deposition and patterning of boron and phosphorus doped CVD oxide films and the diffusion of the doping atoms to form the n+ and p+ regions of the electronic devices.

Membrane, metallization and passivation

The second part starts with the growth of a thermally gate oxide (100 nm) followed by the deposition of a low-stress silicon rich nitride LCPVD film. Then, the gate and contacts are defined in the nitride. The metallization is deposited by e-beam evaporation of aluminum, which is annealed to form ohmic contacts on silicon. A PECVD reactor is used to deposit a silicon nitride passivation layer on the device. After the patterning of the passivation film, thin catalytic metals (CM : Pt, Ir, Pd) are deposited, patterned and annealed. GasFETs with 4 different catalytic metals can be fabricated or one of them can be coated by aluminum and used as a reference. Since the deposition of the CM layers is done prior to the bulk silicon micromachining, a chuck is used in the third and last part of the processing to protect the front side of the wafer during the back side etching of silicon in KOH.

Silicon bulk micromachining

Firstly, the silicon island is defined and protected by the thermally grown oxide film during the etching of 10 μm of silicon in standard KOH (40% at 60°C) to define the silicon island thickness. Secondly, after the removal of the protective oxide, the silicon is entirely etched by using 52% KOH (solubility limit of KOH in water at room temperature) at 70°C. KOH with a concentration of 52% is used to decrease the etch rate of the (311) planes, forming the side of the silicon island, compared to the etch rate of the (100) plane, which is the plane forming the bottom of the silicon island. The ratio between the etch rates in the direction parallel and perpendicular <100> to the wafer surface is about 1.4 for this specific KOH solution.

Despite the fact that the nitride and oxide layers used as membrane are selective to KOH, the release of membrane has to be done with a precise time control of the silicon etching rate to obtain the desired silicon island thickness. Double-face polished wafers with a TTV (Total Thickness Variance) as low as possible are needed since the uniformity of the silicon islands thickness on the entire wafer depends on this parameter.

The whole fabrication process includes 50 steps, 15 of which are photolithographies (12 masks). The fabrication process is compatible with the use of different gate insulators as silicon

dioxide (SiO_2), silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3) and tantalum oxide (Ta_2O_5).

CHARACTERIZATION

Electrical characterizations of MOSFETs designed for this low-power device have shown that they are suitable for gas sensing at temperature up to 225°C. At this maximum operating temperature, a constant current bias of at least 200 μA is needed between the source and drain (connected to the gate) to avoid the interference of leakage currents. Bulk devices coated with thin CM layers (Ir and Pt) show a good sensitivity to H_2 and NH_3 at an operating temperature of 140°C (*Fig. 4*).

The heater resistance value is 1175 Ω ± 30% and decreases as a function of temperature with the behaviour expected for a semiconductor. Power consumption of the device has been evaluated by using the diode previously calibrated as a function of temperature. A low power consumption of 80 mW is achieved for an operating temperature of 175°C for the array of 4 GasFETs compared to 0.5-1.0 W for one standard GasFET

The silicon island ensures a uniform temperature distribution all over the active area. The low thermal mass allows the operation of the sensor in a temperature cycling mode, which enhances the power consumption of the device and could influence the selectivity as in resistive gas sensors.

CONCLUSIONS

The design, fabrication and characterization of a low-power consumption MOSFETs array gas sensor have been presented. The sensor consists of a heating resistor, a diode temperature sensor and 4 GasFETs located in a silicon island thermally isolated from the chip frame by a dielectric membrane. The combination of microelectronics and MEMS (silicon bulk micro-machining) fabrication technologies was used to fabricate these devices. The array of 4 GasFETs has a low-power consumption of 80 mW at an operating temperature of 175°C. The silicon island also provides a uniform temperature all over the sensing area. The low thermal mass of the device allows the operation of the sensors in a temperature cycling mode.

Even if above and in the drawings the island has been described and shown without semiconductor (for instance) silicon in the membrane connection with the support, the membrane may comprise silicon without loss of thermal isolation. The silicon in the membrane may be thin. shaped as spokes or low-doped or even undoped or combinations thereof rendering the thermal

losses through the silicon small.

Claims

1. Micro-hotplate device with integrated chemical sensor, which comprises:

a) a support substrate;

b) a supported membrane, attached to said support substrate, extending over a well in said support substrate;

c) an island attached to said membrane so as to be electrically and thermally isolated from said substrate, said island consisting at least partly of a semiconducting material;

d) one or several heating elements integrated in said island;

e) one or several temperature-sensing elements integrated in said island;

f) one or several active microelectronic devices integrated in said island, where at least one of said active microelectronic devices is a chemical sensor whose chemically active layer is exposed to the ambient.

2. A micro-hotplate device according to claim 1, wherein at least one heating element consists of a heating transistor.

3. A micro-hotplate device according to claim 1, wherein at least one heating element consists of a heating resistor.

4. A micro-hotplate device according to any of the claims 1-3, wherein at least one temperature-sensing element is a temperature-sensitive resistor.

5. A micro-hotplate device according to any of the claims 1-3, wherein at least one temperature-sensing element is a temperature-sensitive diode.

6. A micro-hotplate device according to any of the claims 1-5, wherein said membrane consists of one or several insulator layers.

7. A micro-hotplate device according to claim 6, wherein at least one insulator is silicon nitride.

8. A micro-hotplate device according to claim 6 or 7, wherein electrically conducting leads to the active microelectronic devices on the island have been placed between different insulator layers.

9. A micro-hotplate device according to any of the claims 1-8, wherein the semiconducting material in the island is silicon.

10. A micro-hotplate device according to any of the claims 1-8, wherein the semiconducting material in the island is silicon carbide.

11. A micro-hotplate device according to any of the claims 1-10, wherein the support

substrate and the island are made of the same material.

12. A method for the fabrication of a micro-hotplate device according to claim1, **characterized in** the use of a combination of masking steps and etching steps to define the geometry of the device.

13. A method according to claim 12, **characterized in** the use of consecutive backside etching steps comprising:

a) depositing the supporting membrane over the silicon substrate;

b) one etching step is used to define the thickness of the island by etching away the region surrounding the island to a certain wanted depth, equal to the wanted thickness of the island;

c) another etching step is used to etch the island and surrounding region until the island is isolated from the support substrate.

14. A method according to claim 12, **characterized in** the use of a silicon-on-insulator wafer as substrate whereby the buried insulator layer in said silicon-on-insulator wafer is used as an etch stop to define the thickness of the island of the device, resulting in a silicon island with an insulator layer on backside.

15. A method according to claim 14, **characterized in** the use of the following steps:

a) etching away from the front side of the device the region surrounding the island down to the buried insulator layer;

b) etching away from the back side of the device the silicon in the region below the island and the region surrounding the island until the buried insulator layer on the island is exposed and the island is attached to the support by the insulator layer.

16. A method according to claim 14, **characterized by** the following steps:

a) oxidizing the silicon layer on the front side of the device down to the buried insulator layer, except for the region where the island should be;

b) etching away from the front side of the device the oxide in the region surrounding the island until the underlying silicon substrate is exposed;

c etching away from the back side of the device the silicon in the region below the island until the buried insulator layer on the island is exposed and the island is attached to the support by the remaining part of the insulator layer.

17. A method according to any of the claims 12-16, wherin at least one of said etching steps is an anisotropic potassium hydroxide etching step.

18. A method according to any of the claims 12-16, wherein at least one of said etching

steps is an anisotropic tetramethyl ammonium hydroxide etching step.

19. A method according to any of the claims 12-16, at least one of said etching steps is a deep reactive ion etching step.

20. A micro-hotplate device according to any of the claims 1-12, wherein one or several of the chemical sensors utilize the field-effect detection mechanism.

21. A micro-hotplate device according to claim 20, wherein one or several field-effect chemical sensors are combined with one or several chemical sensors that utilize a detection mechanism different from the field effect.

22. A micro-hotplate device according to any of the claims 1-12 or 21, wherein one or several of the chemical sensors are operated as gas sensors.

23. A micro-hotplate device according to claims 21 and 22, wherein one or several field-effect gas sensors are combined with one or several gas sensors that utilize resistance changes as detection mechanism.

24. A micro-hotplate device according to claim 23, wherein at least one of the gas sensors that utilize resistance changes as detection mechanism is made of a semiconducting metal oxide.

25. A micro-hotplate device according to claim 23, wherein at least one of the gas sensors that utilize resistance changes as detection mechanism is made of a polymer.

26. A micro-hotplate device according to any of the claims 1-12 or 20-25, wherein the support substrate contains an array of several islands.

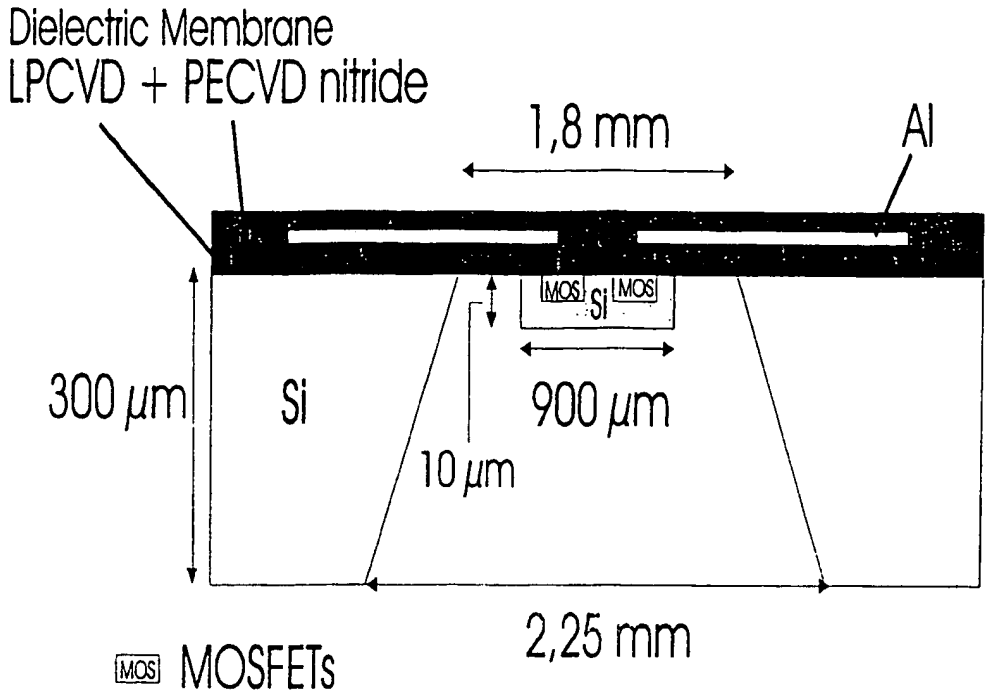
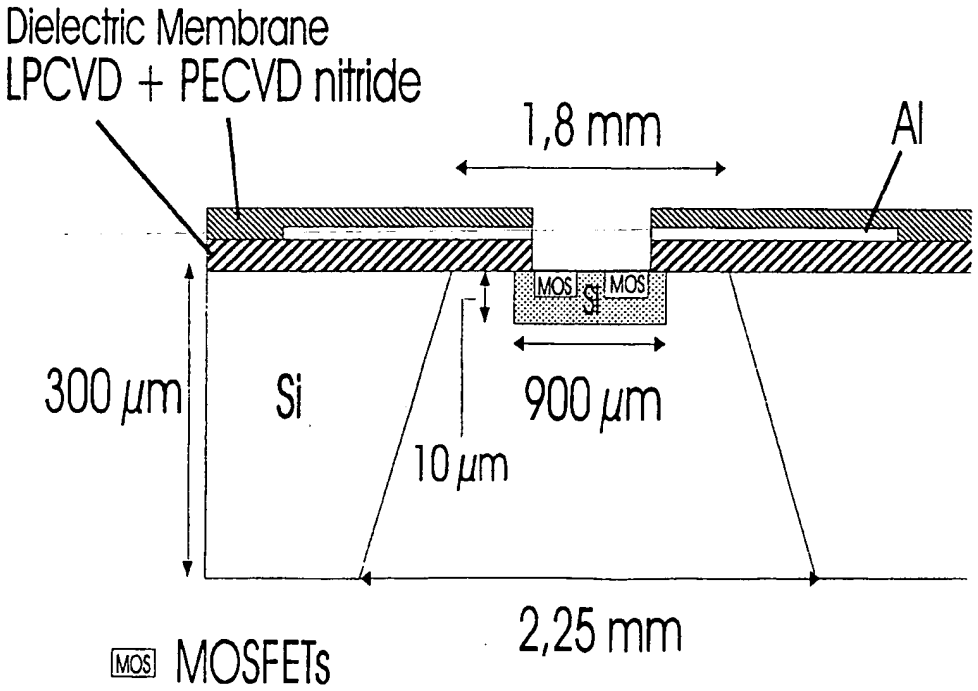

Dielectric Membrane
LPCVD + PECVD nitride
1,8 mm
Al
MOS Si MOS
300 µm
Si
900 µm
10 µm
2,25 mm
MOS MOSFETs

Fig 1


Dielectric Membrane
LPCVD + PECVD nitride
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Al
MOS Si MOS
300 µm
Si
900 µm
10 µm
2,25 mm
MOS MOSFETs

Fig 5

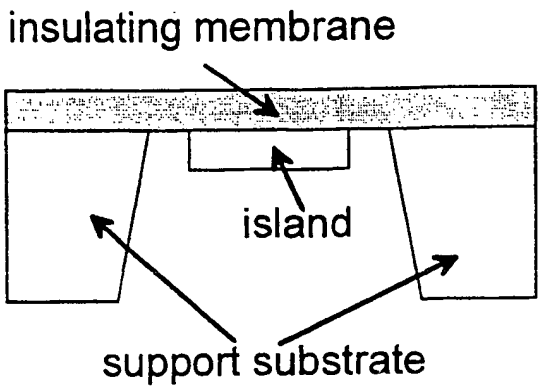

Fig 2

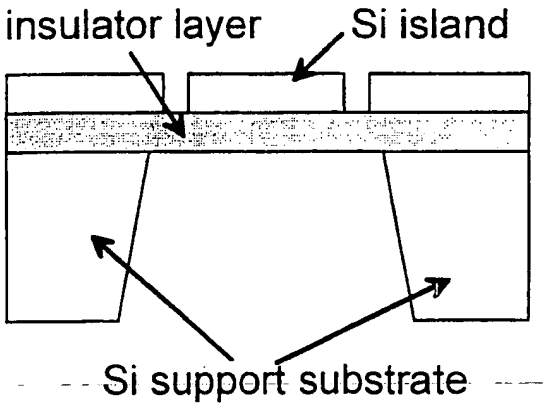

Fig 3

Fig 3

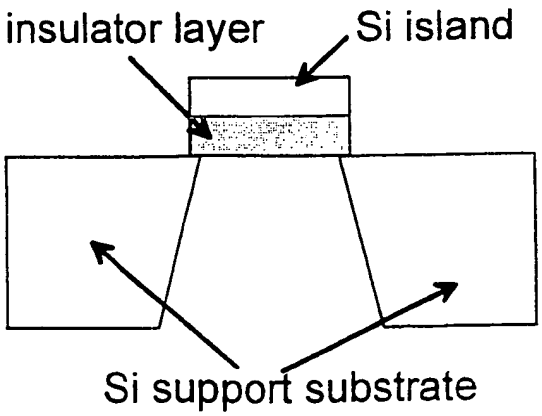

Fig 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 00/01134

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: G01N 27/414, G01N 27/18
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: G01N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 9410822 A1 (THE UNITED STATES OF AMERICA AS REPRESENTED BY THE UNITED STATES DEPARTMENT OF COMMERCE), 11 May 1994 (11.05.94), page 8, line 2 - line 3; page 3, line 18 - page 4, line 20, figure 5 --	1-26
X	WO 9410821 A1 (UNITED STATES OF AMERICA, AS REPRESENTED BY THE UNITED STATES DEPARTMENT OF COMMERCE), 11 May 1994 (11.05.94), abstract --	1-26

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 Sept 2000	09 -10- 2000
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Moa Grönkvist/ELY Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

Information on patent family members

01/08/00

International application No.
PCT/SE 00/01134

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9410822 A1	11/05/94	US 5464966 A	07/11/95
WO 9410821 A1	11/05/94	AU 5450194 A	24/05/94
		US 5356756 A	18/10/94